WHAT IS CLAIMED IS:

1. A circuit having a plurality of stages, each stage comprising:

a first logic circuit;

a latch coupled to a second logic circuit of an adjacent stage;

a switch which connects the first logic circuit to the latch in a first state and disconnects the logic circuit from the latch in a second state; and

a local clock circuit which controls the first and second states by providing a locally generated clock signal to activate the switch, the locally generated clock signals being generated by interlocking handshake signals from a local clock circuit of an adjacent stage.

2. The circuit as recited in claim 1, wherein the interlocking handshake signals include an acknowledge signal from a downstream local clock circuit and a valid signal from an upstream local clock circuit such that when one stage is enabled immediately adjacent stages are disabled for data transfer in a current clock cycle.

3. The circuit as recited in claim 1, wherein the local clock circuit outputs the locally generated clock responsive to the acknowledge signal and the valid signal.

4. The circuit as recited in claim 1, wherein the interlocking handshake signals guarantee that when a current latch is enabled a latch of a previous stage and a latch of subsequent stage are disabled.

5. The circuit as recited in claim 1, wherein the local clock circuit for each stage is enabled only when there is an operation to perform.

6. The circuit as recited in claim 1, wherein each stage includes a scan chain which permits data to be input and output to each stage in accordance with an external clock.

7. The circuit as recited in claim 1, wherein the latch includes a first end connected to the switch and a second end connected to a data scan latch, the data scan latch connecting the second end of the latch to a first end

of a next corresponding latch of an adjacent stage such that data is scanned into or out of the latch through the data scan latch.

8. The circuit as recited in claim 1, wherein the circuit includes an asynchronous pipeline.

9. A method for transferring data in an interlocked pipeline circuit having a plurality of stages, comprising the steps of:

providing, for each stage, a latch connected to an input of that stage and a switch for selectively coupling the input of the stage to an output of the previous stage;

when the data is valid in a current stage, sending a valid signal to a local clock circuit of a next stage of the plurality of stages;

sending an acknowledge signal from the local clock circuit of the next stage to a local clock circuit of the current stage responsive to the valid signal;

generating a local clock signal at the local clock circuit of the current stage of the plurality of stages based on the acknowledge signal and the valid signal; and

enabling the switch of the current stage based on the local clock signal to permit data transfer to the latch of the current stage from the output of the previous stage.

10. The method as recited in claim 9, further comprising the step of interlocking the local clock circuits such that when one stage is enabled immediately adjacent stages are disabled for data transfer in a current clock cycle.

11. The method as recited in claim 9, further comprising the step of disabling the switch of the current stage during operations of an adjacent stage.

12. The method as recited in claim 9, wherein the step of generating a local clock signal at the local clock circuit of the current stage includes enabling the local clock circuit for each stage only when there is an operation to perform.

13. The circuit as recited in claim 9, wherein each stage includes a scan chain which permits data to be input

and output to each stage in accordance with an external clock.

14. The method as recited in claim 9, wherein the latch of the current stage includes a first end connected to the switch and a second end connected to a data scan latch, the data scan latch connecting the second end of the latch to a first end of a next corresponding latch of an adjacent stage, the method further comprising the step of scanning data into or out of the latch through the data scan latch.

15. The method as recited in claim 14, further comprising the step of selectively enabling the switches to perform data scanning.